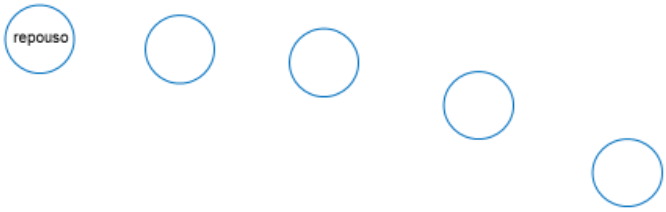
Circuitos Lógicos

Módulo # 5

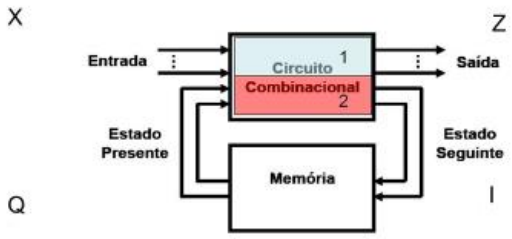
Circuitos Sequenciais

Projetar um circuito que implemente o segredo eletrônico para este cofre

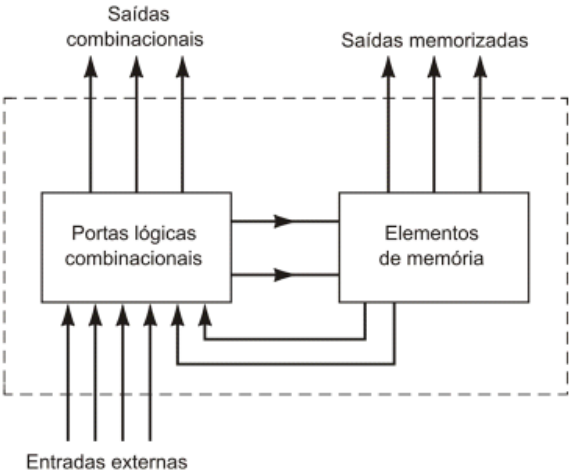
Por exemplo, que o segredo seja **5379** , fixo.
Vamos descrever seu funcionamento, passo-a-passo ...



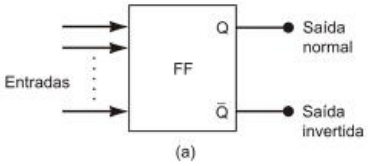
Circuito Sequencial : blocos funcionais



Circuito Sequencial : blocos funcionais



Elemento de memória : flip-flop genérico



(a)

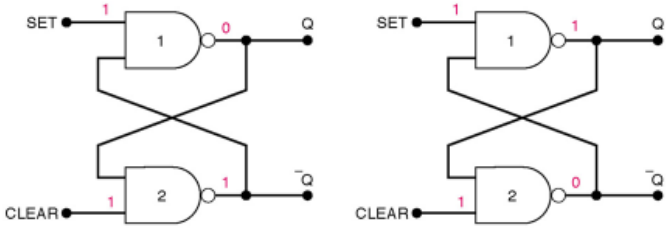
Estados de saída

$Q = 1, \bar{Q} = 0$: denominado estado ALTO ou 1; também chamado de estado SET

$Q = 0, \bar{Q} = 1$: denominado estado BAIXO ou 0; também chamado de estado CLEAR ou RESET

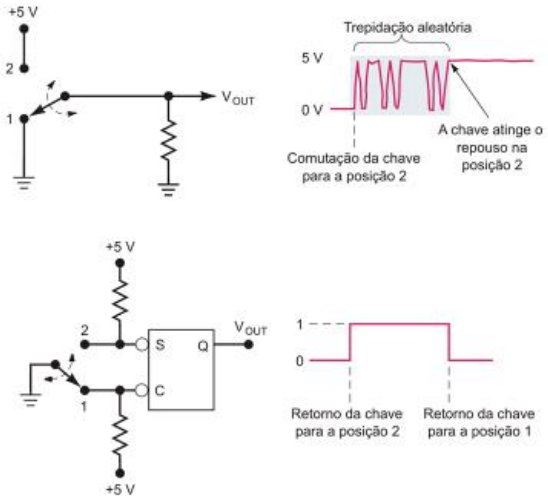
(b)

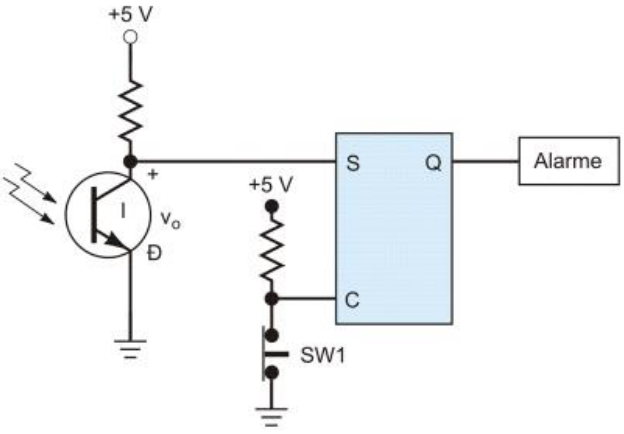
Flip-flop RS com NANDs



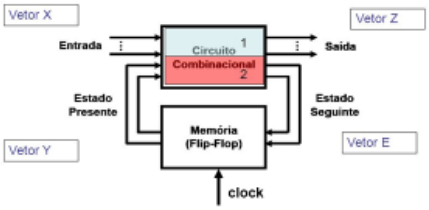
Set	Clear	Saída
1	1	Não muda
0	1	Q = 1
1	0	Q = 0
0	0	Inválida*

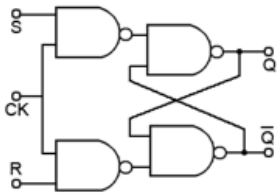
*Produz $Q = \bar{Q} = 1$

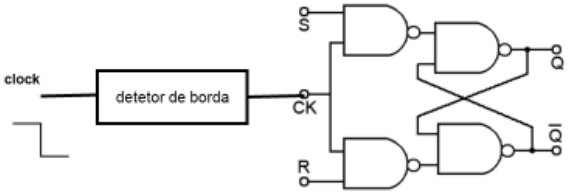

+5 V
2
1
V_{OUT}
Trepidação aleatória
5 V
0 V
A chave atinge o repouso na posição 2
Comutação da chave para a posição 2
+5 V
2
1
S
Q
C
V_{OUT}
+5 V
1
0
Retorno da chave para a posição 2
Retorno da chave para a posição 1

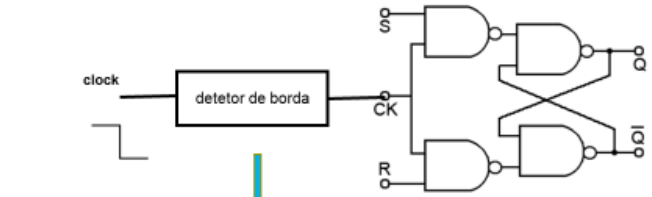

+5 V
+
I
V_O
Đ
+5 V
S
Q
Alarme
C
SW1

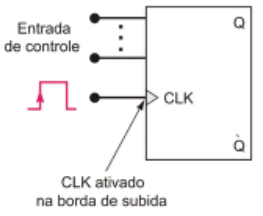
Circuitos Sequenciais Síncronos ou FMS

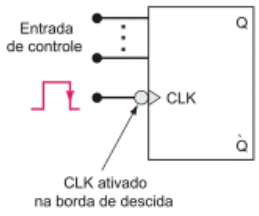


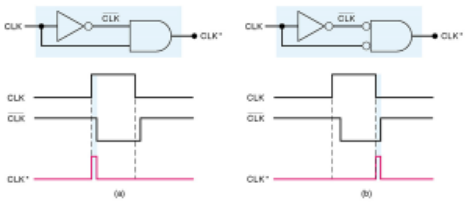




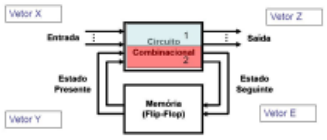




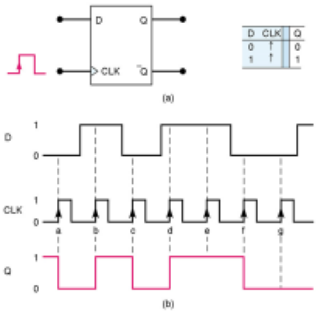


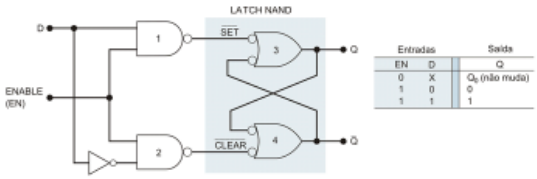


Circuitos Sequenciais Síncronos ou FMS



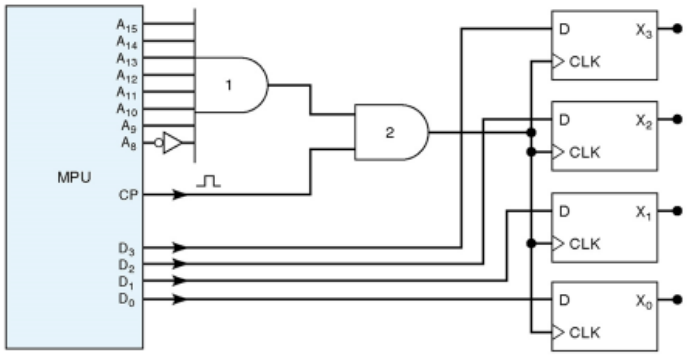
Flip-flop tipo D





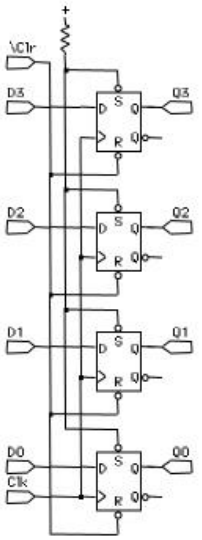
Entradas		Saída
EN	D	Q
0	X	Q_0 (não muda)
1	0	0
1	1	1

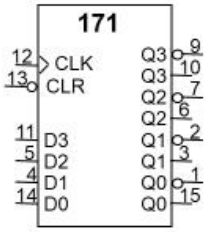
Aplicações do FFP-D

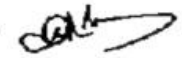


Aplicações do FFP-D

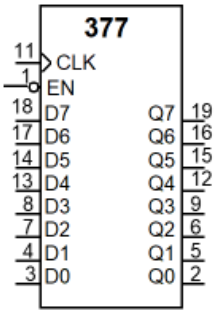
TTL 74171 Quad D-type FF with Clear

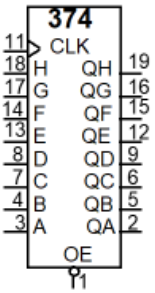






Aplicações do FFP-D



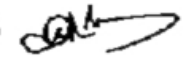


74377 Octal D-type FFs with input enable

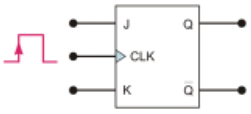
EN enabled low and lo-to-hi clock transition to load new data into register

74374 Octal D-type FFs with output enable

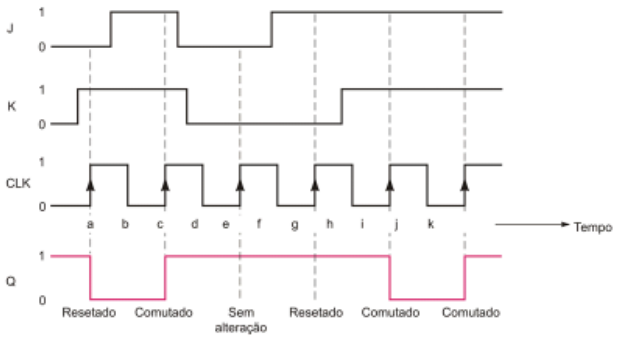
OE asserted low presents FF state to output pins; otherwise high impedence



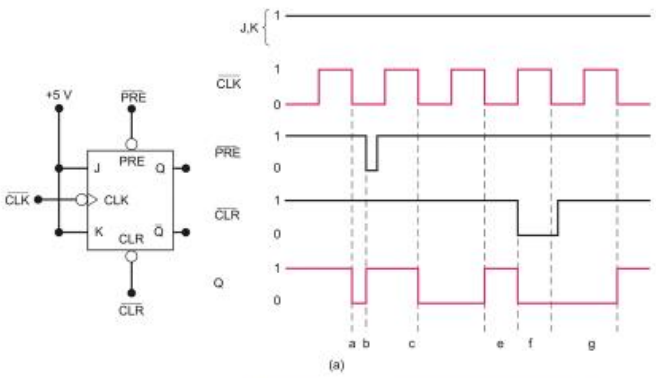
Flip-flop JK



J	K	CLK	Q
0	0	_	Q_0 (não muda)
1	0	_	1
0	1	_	0
1	1	_	$\bar{Q}_0$ (comuta)



Flip-flop JK

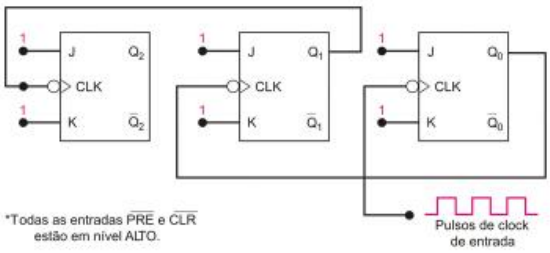


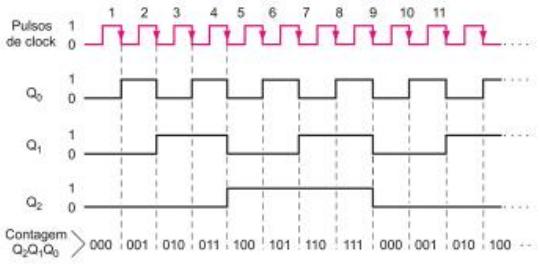
(a)

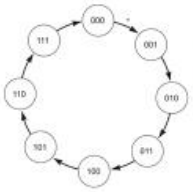
Ponto	Operação
a	Comutação sincronizada na borda de descida de $\overline{CLK}$
b	Q é assincronamente colocada em 1 quando $\overline{PRE}$ = 0
c	Comutação síncrona
d	Comutação síncrona
e	Q é assincronamente colocada em 0 quando $\overline{CLR}$ = 0
f	$\overline{CLR}$ se sobrepõe à borda de descida de $\overline{CLK}$
g	Comutação síncrona

(b)

Função TOGGLE : principal aplicação

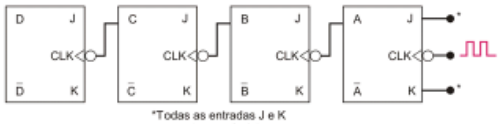


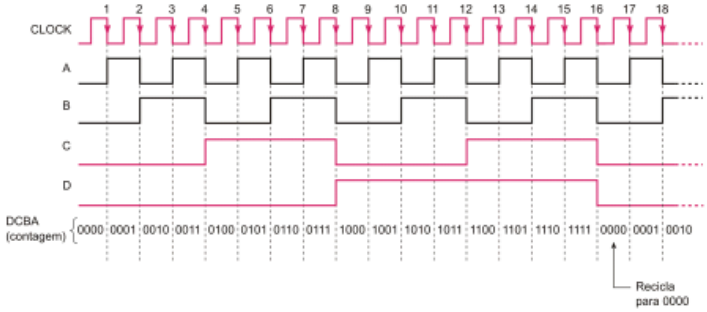




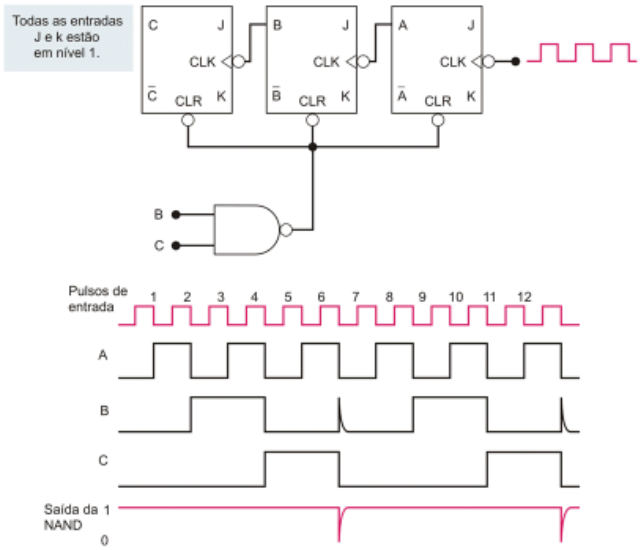
* Nota: cada seta representa a ocorrência de um pulso de clock

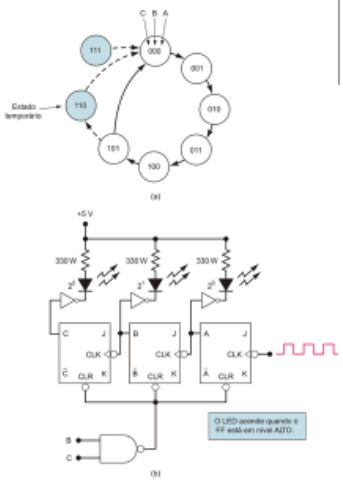
Contador módulo 16





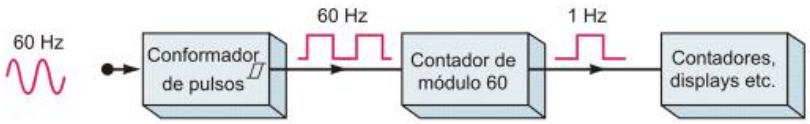
Contador módulo ≠ potência de 2



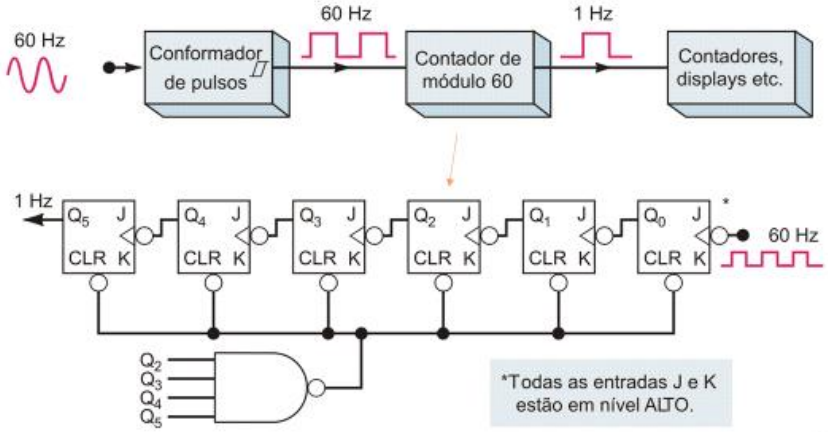


Desafio : projetar um relógio digital.

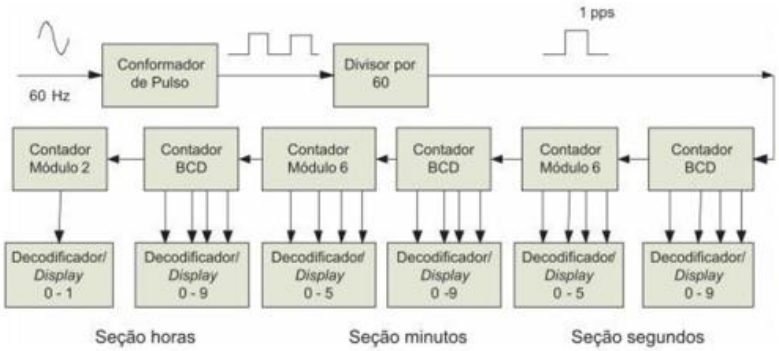
Sugestão para o clock padrão



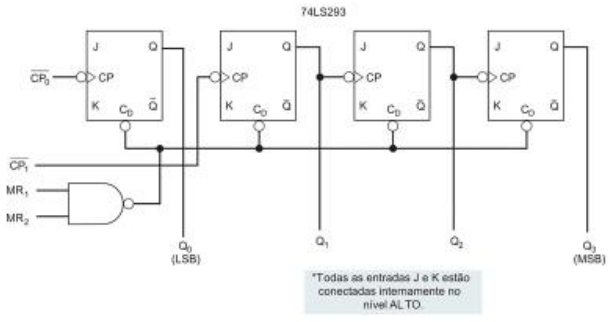
$60_{10} = 11110_2$

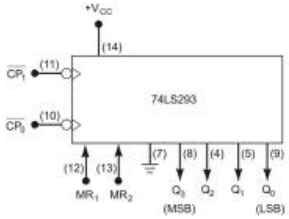


Desafio : projetar um relógio digital.



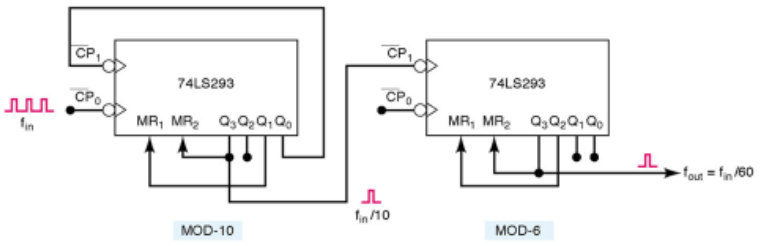
Contador assíncrono 74LS293





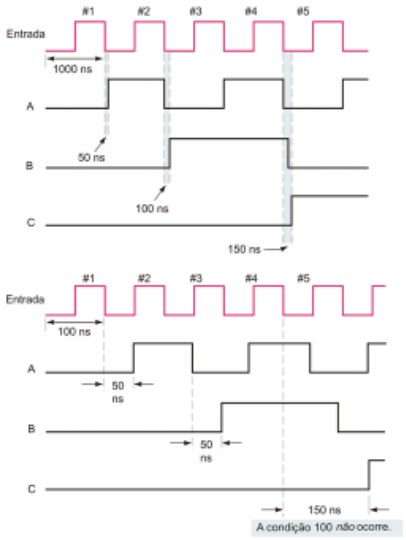
Contador assíncrono 74LS293

Contador módulo 60

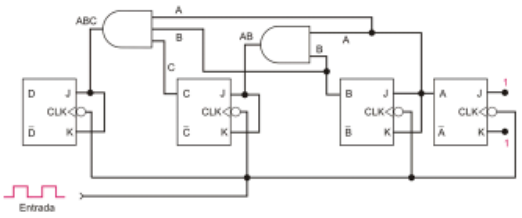


Contador assíncrono : limitações ...

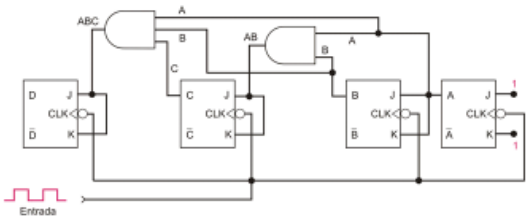
Formas de onda de um contador de três bits ilustrando os efeitos dos atrasos de propagação dos FFs para diferentes freqüências de pulsos de entrada.



Contador assíncrono : limitações ... solução

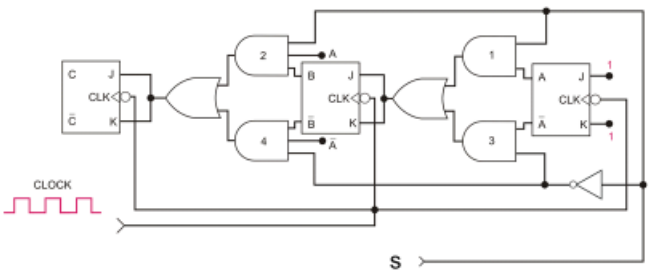


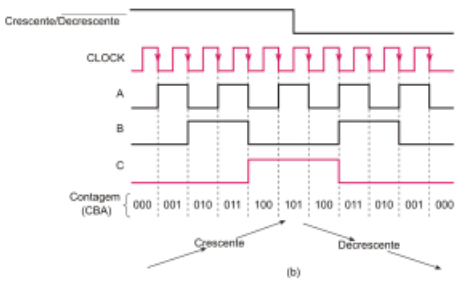
Contador assíncrono : limitações ... exemplo-solução



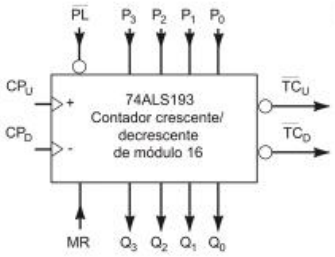
Contagem	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0
.	.	.	.	.
.	.	.	.	.
.	.	etc.	.	.

Analisar o circuito





Contador 74ALS193



Pino	Descrição
CP_U	Entrada de clock para contagem crescente (ativo na borda de subida)
CP_D	Entrada de clock para contagem decrescente (ativo na borda de subida)
MR	Entrada assíncrona de reset geral (ativa em nível ALTO)
$\overline{PL}$	Entrada assíncrona de carga paralela (ativa em nível BAIXO)
P_0- P_3	Entrada de dados em paralelo
Q_0- Q_3	Saídas dos flip-flops
$\overline{TC_D}$	Saída de contagem terminal decrescente (empréstimo) (ativa em nível ALTO)
$\overline{TC_U}$	Saída de contagem terminal crescente (carry) (ativa em nível ALTO)

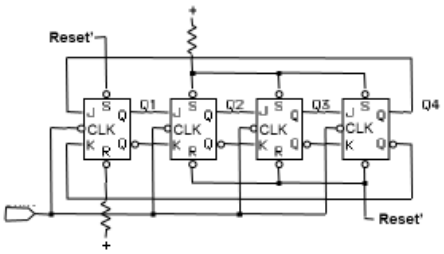
Seleção do Modo de Operação

MR	$\overline{PL}$	CP_U	CP_D	Modo
H	X	X	X	Reset assíncrono
L	L	X	X	Preset assíncrono
L	H	H	H	Não muda
L	H	⎍	H	Contagem crescente
L	H	H	⎍	Contagem decrescente

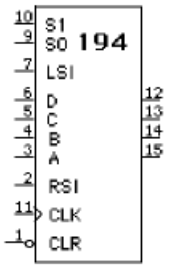
H = HIGH = AL TO; L = LOW = BAIXO
X = Não importa (don't care); ↑ = Transição positiva

Aplicações com flip-flops

Após sinal de Reset, são aplicados sucessivos pulsos de clock.
Qual será a resposta desse circuito, tendo como saída o estado do mesmo ?



CI 74194

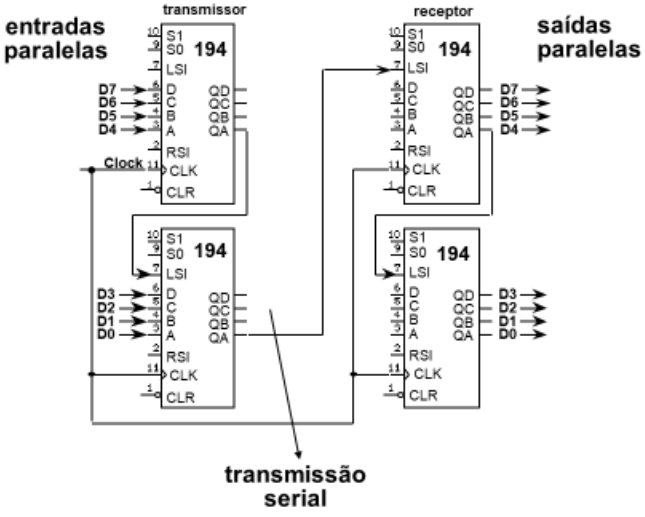


Serial Inputs: LSI, RSI
Parallel Inputs: D, C, B, A
Parallel Outputs: QD, QC, QB, QA
Clear Signal
Positive Edge Triggered Devices

S1,S0 determine the shift function
S1 = 1, S0 = 1: Load on rising clk edge synchronous load
S1 = 1, S0 = 0: shift left on rising clk edge LSI replaces element D
S1 = 0, S0 = 1: shift right on rising clk edge ;RSI replaces element A
S1 = 0, S0 = 0: hold state

Aplicações com flip-flops : shift register

Conversão paralela - serial - paralela



Leitura indicada

Maini, A.K. “Digital Electronics – Principles and Integrated Circuits”

a) Sec. 8.3 – 8.11 , pgs. 284 – 311

b) Sec. 9.1 – 9.13 , pgs. 317 – 360

8 Flip-Flops and Related Devices

LEARNING OBJECTIVES

After completing this chapter, you will learn the following:

- Operational basics of bistable, monostable, and astable multivibrators.
- Digital and linear integrated circuits for implementing multivibrator functions.
- Operational basics of *R-S*, *J-K*, toggle, and *D* flip-flops.
- Use of *J-K* flip-flop to construct other flip-flops.
- Timing parameters of flip-flops.
- Applications of flip-flops.
- Application-relevant data on commonly used flip-flops and related devices.

9 Counters and Registers

LEARNING OBJECTIVES

After completing this chapter, you will learn the following:

- Difference between asynchronous (or ripple) and synchronous counters.
- Operational principle of asynchronous and synchronous counters.
- Design methodology for asynchronous and synchronous counters.
- Designing counters with variable modulus.
- Designing counters with arbitrary sequences.
- BCD, decade counters, UP, DOWN, and UP/DOWN counters.
- Counters with PRESET and CLEAR features.
- Cascading counters.
- Decoding counters.
- Operational principle of different types of registers.
- Operational principle and features of register-based counters.
- ANSI representation of counters and registers available in IC form.
- Application-relevant information on counters and registers.