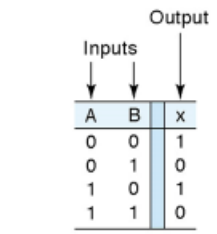
Circuitos Lógicos

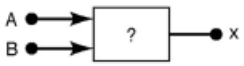
Módulo # 2

Funções e Tecnologias das Famílias Lógicas

Tabelas verdade



A	B	x
0	0	1
0	1	0
1	0	1
1	1	0



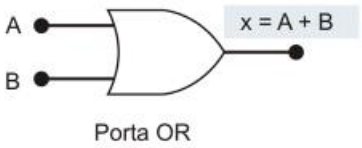
A	B	C	x
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

A	B	C	D	x
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

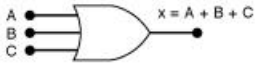
Função OR

OR

A	B	x = A + B
0	0	0
0	1	1
1	0	1
1	1	1

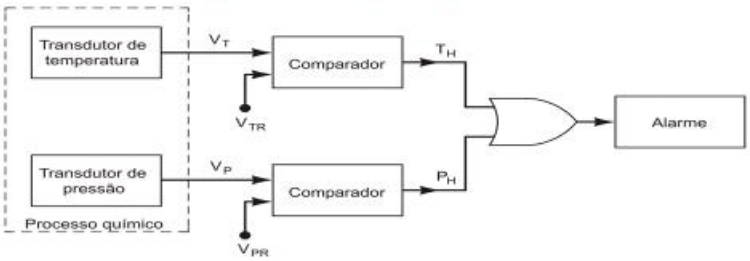


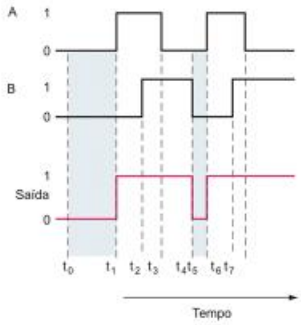
Porta OR

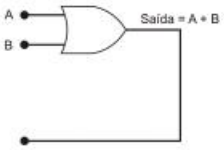


A	B	C	x = A + B + C
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Função OR - aplicações



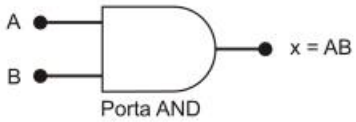




Função AND

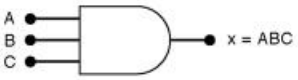
AND

A	B	x = A · B
0	0	0
0	1	0
1	0	0
1	1	1

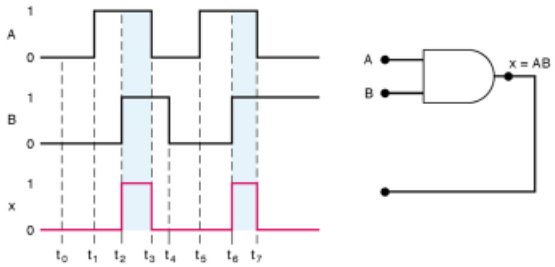


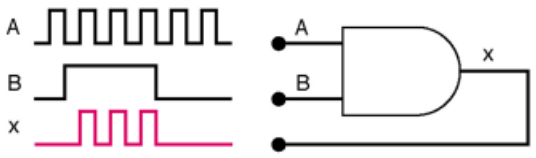
Porta AND

A	B	C	x = ABC
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



Função AND - aplicações

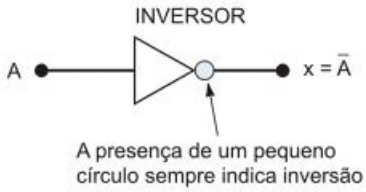


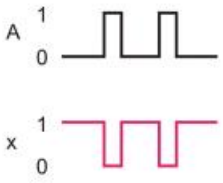


Função INVERSOR - NOT

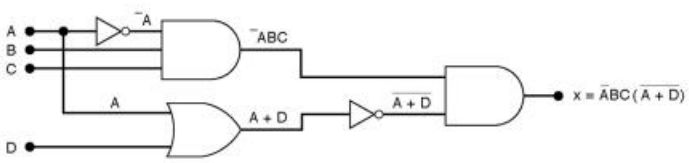
INVERSOR

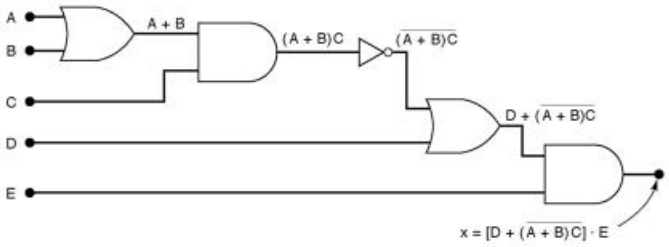
A	x = $\overline{A}$
0	1
1	0



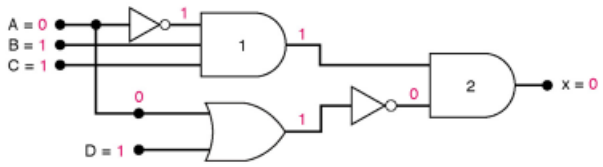


Combinações





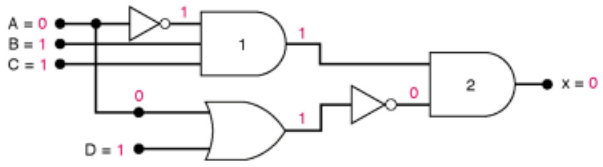
Análise de circuitos



A	B	C	D	X
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	0
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

X = A'.B.C . (A+D)'

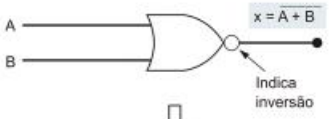
Análise de circuitos

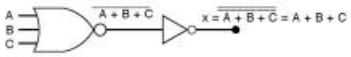


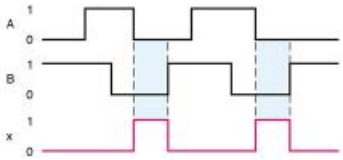
A	B	C	D	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

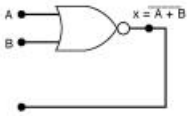
X = A'.B.C . (A+D)'

Função NOR



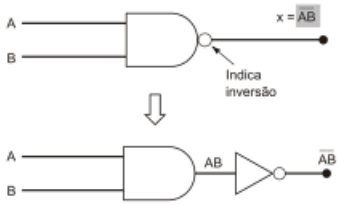






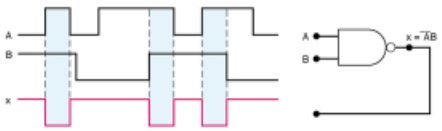
		OR	NOR
A	B	A + B	$\overline{A + B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Função NAND

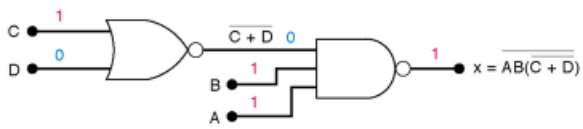


		AND	NAND
A	B	AB	$\overline{AB}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

(c)



Análise de circuitos



A	B	C	D	X
...	...	...	...	
1	1	0	0	
1	1	0	1	
1	1	1	0	1
1	1	1	1	

Função XOR

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

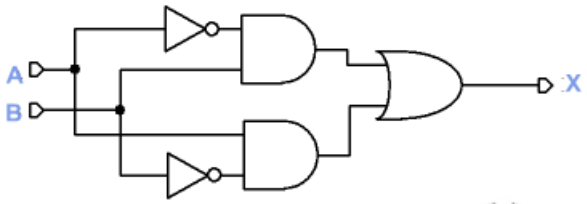
Onde X = 1 ? X = 1 quando :

A = 0 e B = 1 ..... A' . B

Ou ..... +

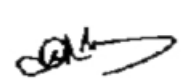
A = 1 e B = 0 ..... A . B'

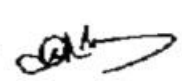
$$X = \overline{A} . B + A . \overline{B}$$

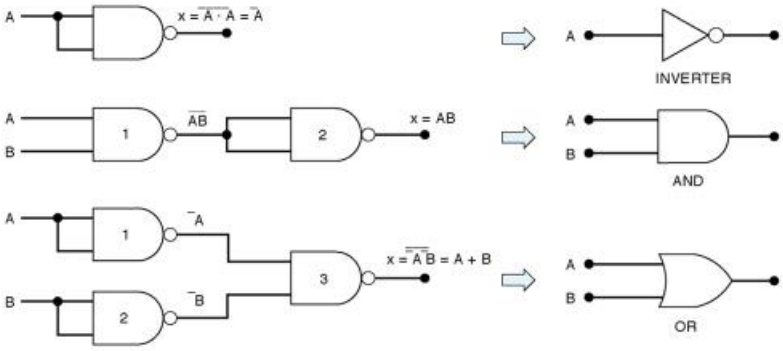


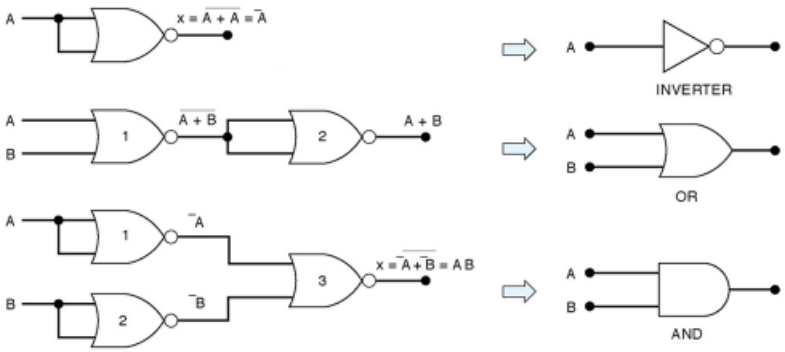
Álgebra de Boole

	Combinações		Propriedades
	OR	**AND**	
1.	$a + b = b + a$	$ab = ba$	**Comutativa**
2.	$a + (bc) = (a + b)(a + c)$	$a(b + c) = (ab) + (ac)$	**Distributiva**
3.	$a + (b + c) = (a + b) + c$	$a(bc) = (ab)c$	**Associativa**
	$= a + b + c$	$= abc$	
4.	$a + a = a$	$aa = a$	
5.	$a + a' = 1$	$aa' = 0$	**Complemento**
6.	$1 + a = 1$	$0a = 0$	
7.	$0 + a = a$	$1a = a$	
8.	$(a')' = a$		
9.	$a + ab = a$	$a(a + b) = a$	
10.	$a + a'b = a + b$	$a(a' + b) = ab$	
11.	$(a + b)' = a'b'$	$(ab)' = a' + b'$	**Teorema de DeMorgan**

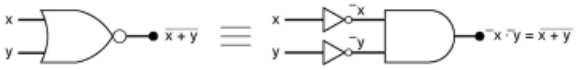




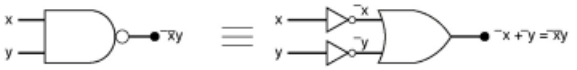

A
x = Ā · A = Ā
A
INVERTER
A
B
1
2
x = AB
A
B
AND
A
B
1
2
3
x = Ā B̄ = A + B
A
B
OR


A
x = Ā + A = Ā
A
INVERTER
A
B
1
2
A + B
A
B
OR
A
B
1
2
3
x = Ā + B̄ = AB
A
B
AND

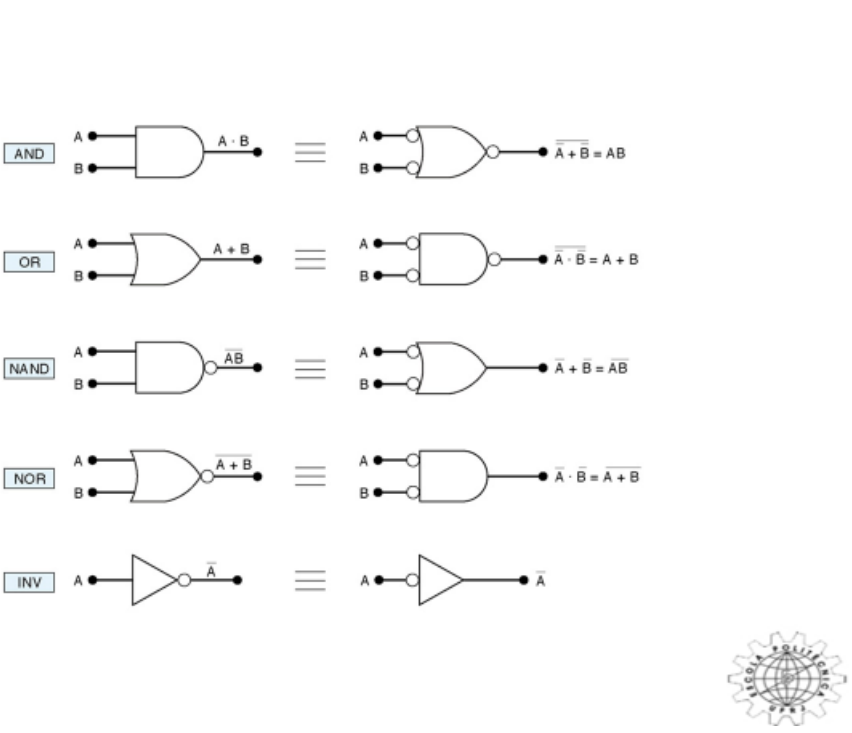
Teorema de DeMorgan



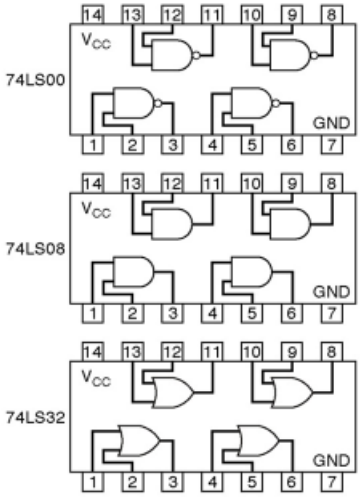
$$\overline{X + Y} = \overline{X} \cdot \overline{Y}$$



$$\overline{X \cdot Y} = \overline{X} + \overline{Y}$$



Circuitos digitais

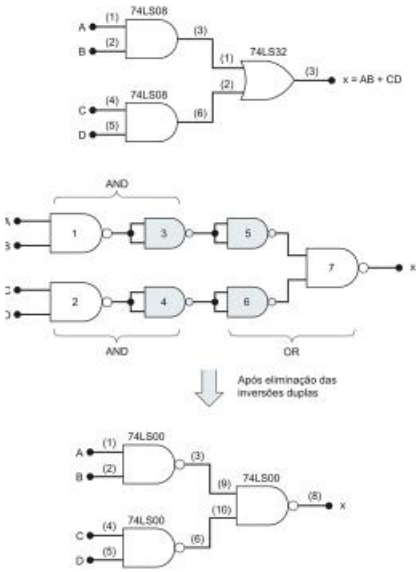


NAND

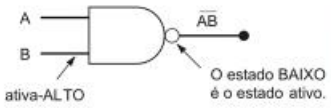
AND

OR

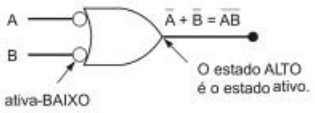
Redução de circuitos



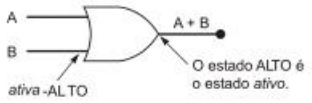
Níveis lógicos



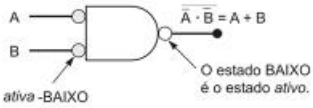
A saída vai para o nível BAIXO apenas quando todas as entradas forem para o nível ALTO.



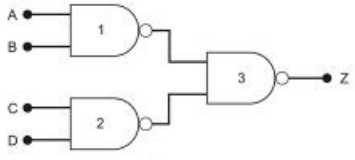
A saída vai para o nível ALTO quando qualquer entrada for para o nível BAIXO.

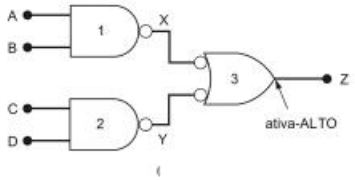


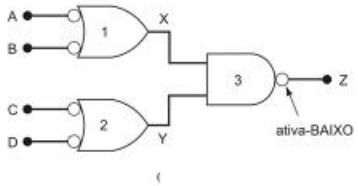
A saída vai para o nível BAIXO quando todas as entradas forem para o nível BAIXO.



A saída vai para o nível ALTO quando qualquer entrada for para o nível ALTO.

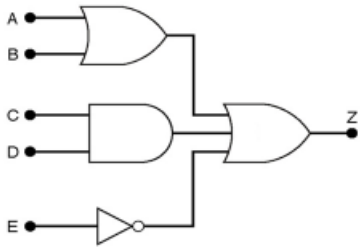


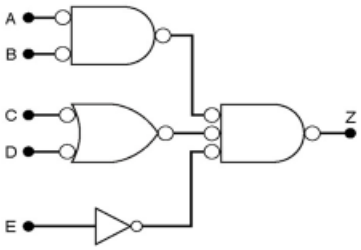


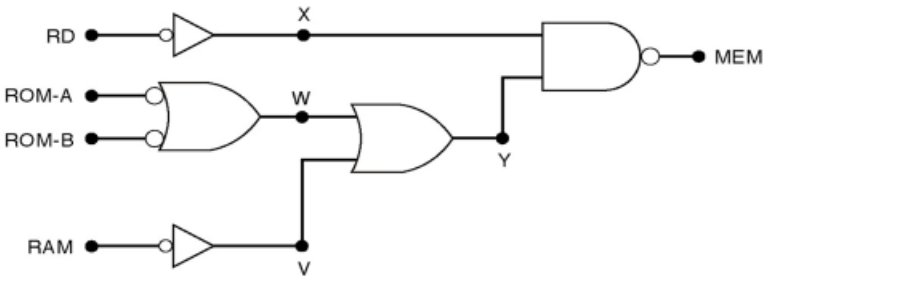


A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Exercícios







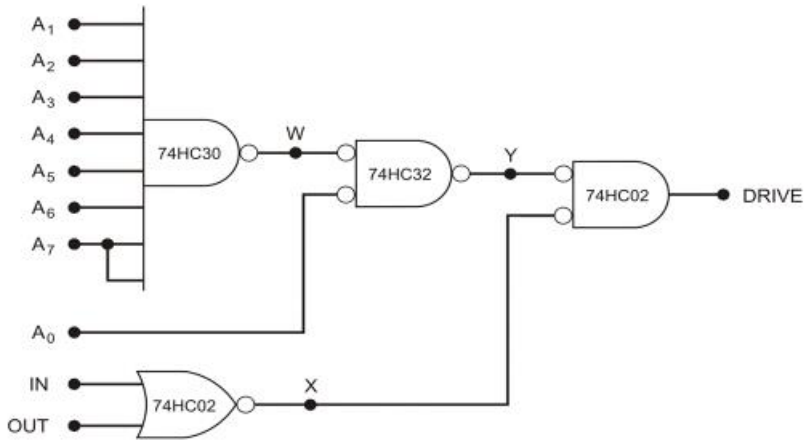
O que se quer representar ?

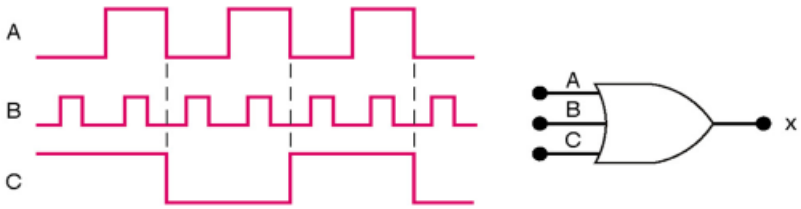
Uma fábrica precisa de uma sirene para indicar final de expediente.

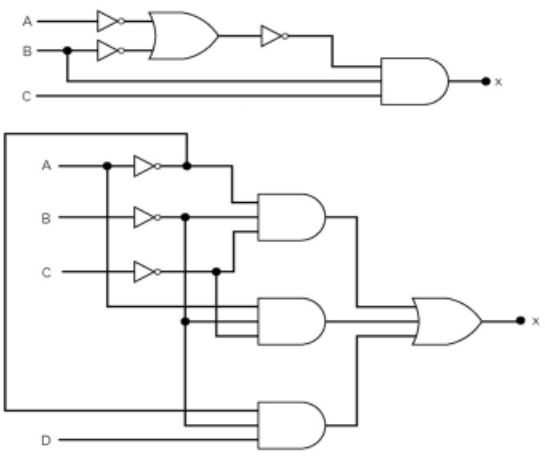
Ela deve ser ativada quando ocorrer uma das seguintes condições:

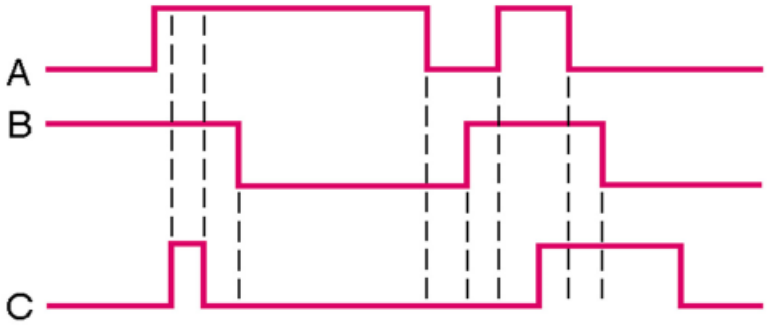
* já passou das 17:00 h e as máquinas estão ligadas ;

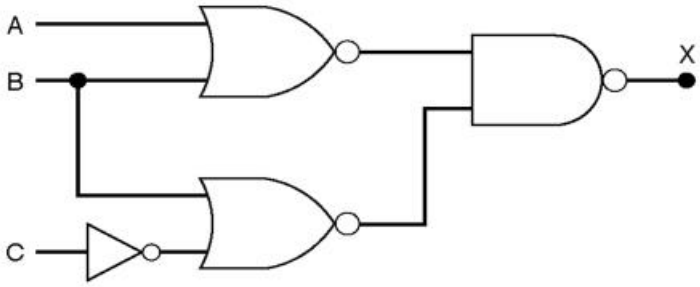
* é sexta-feira, a produção foi atingida e todas as máquinas estão desligadas.

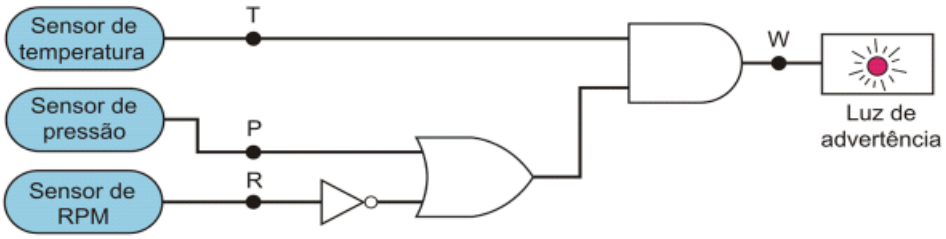


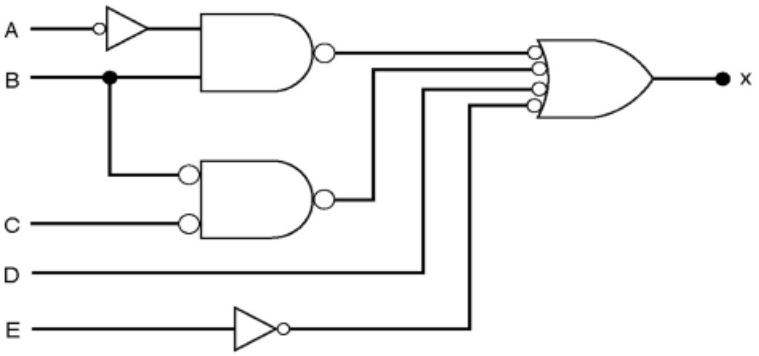

A
B
C
A
B
C
x

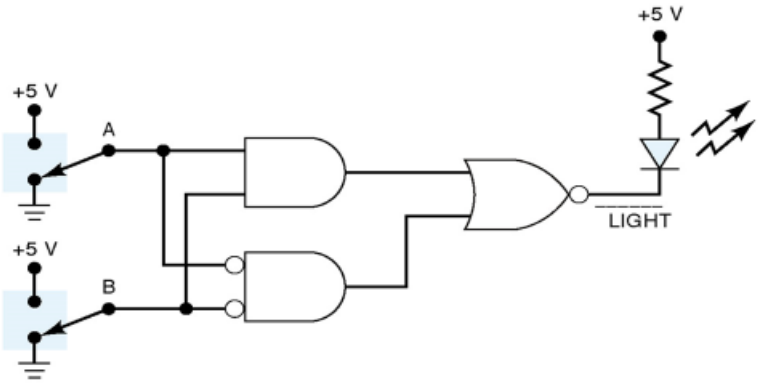

A
B
C
x
A
B
C
x
D


A
B
C


A
B
C
X

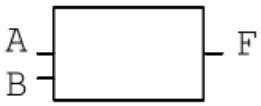

Sensor de temperatura
Sensor de pressão
Sensor de RPM
T
P
R
W
Luz de advertência

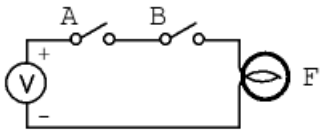

A
B
C
D
E
x


+5 V
A
+5 V
B
+5 V
LIGHT

Famílias Lógicas e a Tecnologias de CIs

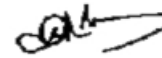
Circuitos lógicos são dispositivos físicos que implementam funções lógicas.



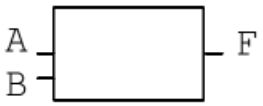


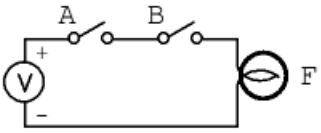
... são 3 variáveis booleanas, ou seja, têm dois "valores físicos" que vão representar o 0 e o 1.

Que função está representada no circuitos elétrico acima ?



Circuitos lógicos são dispositivos físicos que implementam funções lógicas.





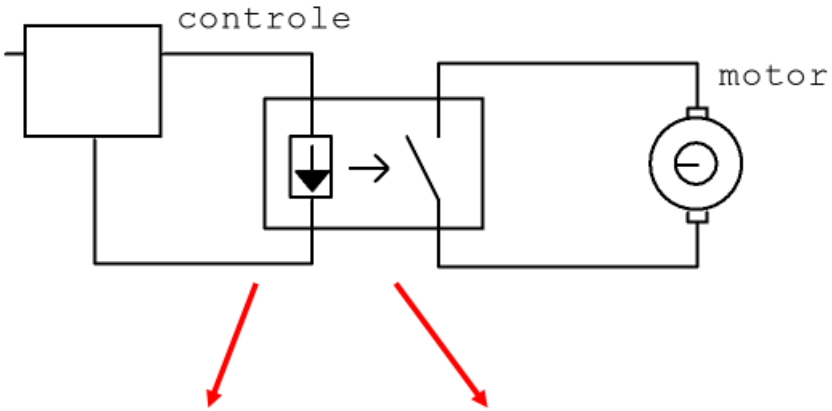
... são 3 variáveis booleanas, ou seja, têm dois "valores físicos" que vão representar o 0 e o 1.

Que função está representada no circuitos elétrico acima ?

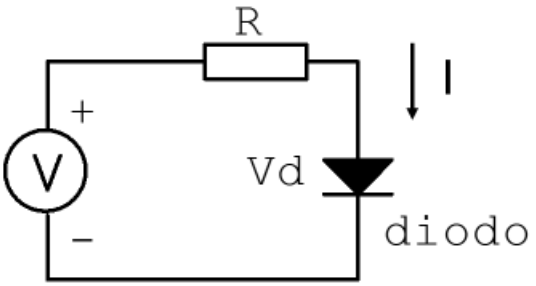
... se A e B	0	aberta
	1	fechada
... se F	0	apagada
	1	acesa

⇨ porta AND

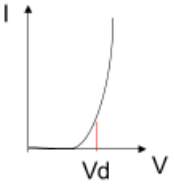
Outro dispositivo ...



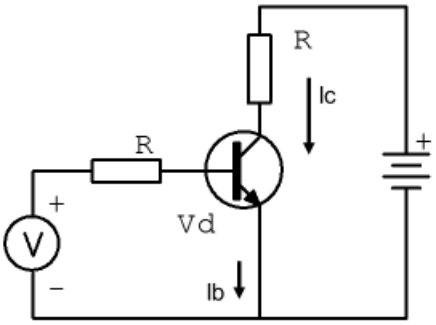
Importantes dispositivos ... diodo



... Se tensão sobre o diodo for Vd, então existe a corrente I.



Importantes dispositivos ... transistor



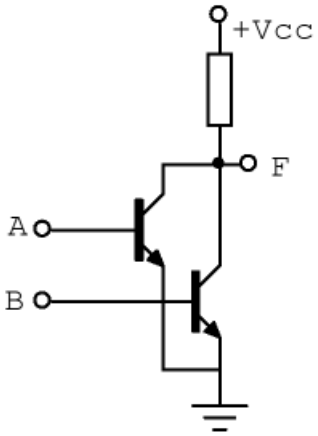
... se tensão sobre a junção PN base-emissor, chamada Vbe for Vd, então existe uma corrente passando nela, chamada Ib; se existe Ib então existe Ic.

... então há duas situações possíveis :

CORTE : Ib = 0 { V = 0 ou Vbe < Vd ⇒ Ic = 0, Vce max

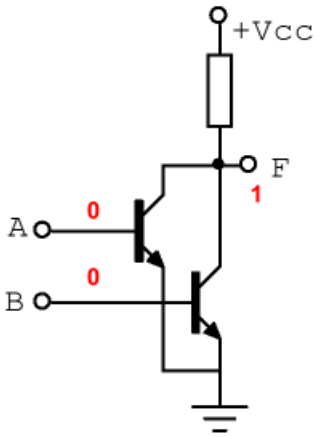
SATURAÇÃO : Ib ≠ 0 { V ≠ 0 e Vbe = Vd ⇒ Ic ≠ 0, Vce min

Vamos analisar o circuito abaixo ...



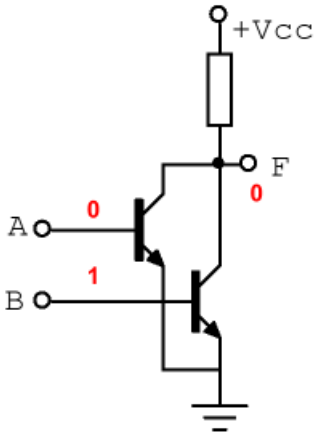
A	B	F
0	0	
0	1	
1	0	
1	1	

Vamos analisar o circuito abaixo ...

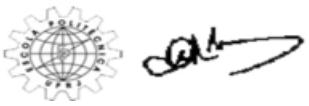


A	B	F
0	0	1
0	1	
1	0	
1	1	

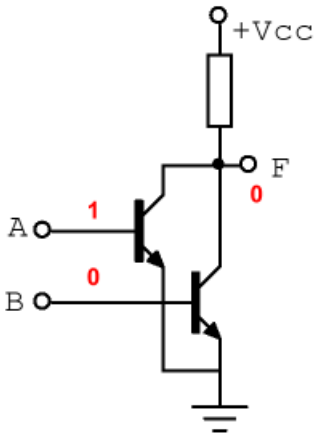
Vamos analisar o circuito abaixo ...



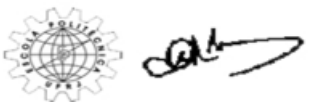
A	B	F
0	0	1
0	1	0
1	0	
1	1	



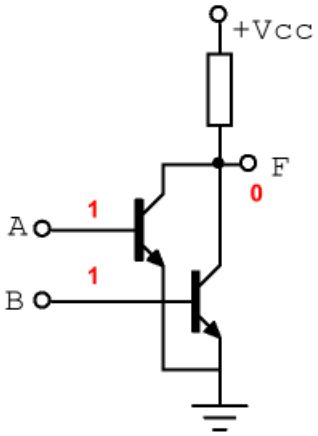
Vamos analisar o circuito abaixo ...



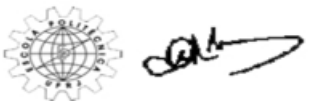
A	B	F
0	0	1
0	1	0
1	0	0
1	1	



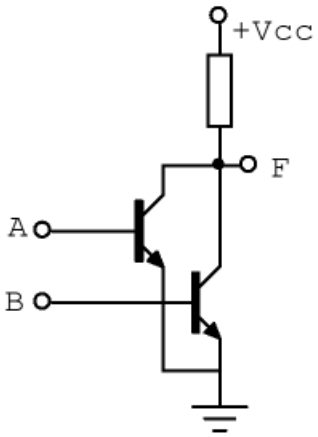
Vamos analisar o circuito abaixo ...



A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

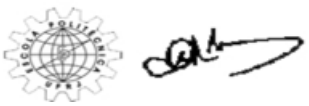


Vamos analisar o circuito abaixo ...

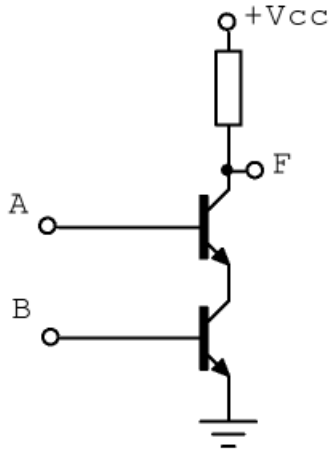


A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

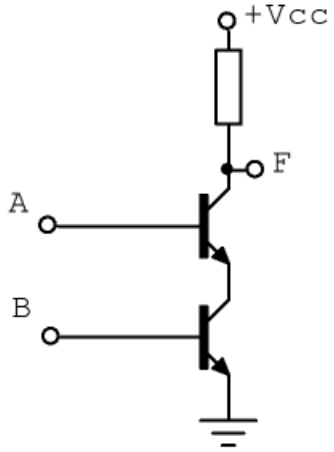
NOR



Vamos analisar o circuito abaixo ...



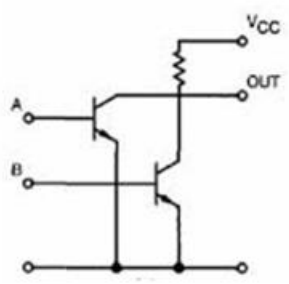
Vamos analisar o circuito abaixo ...



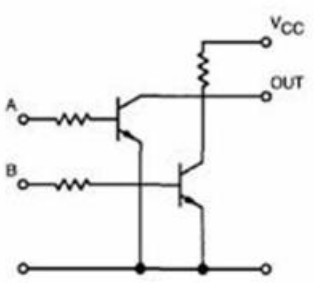
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

NAND

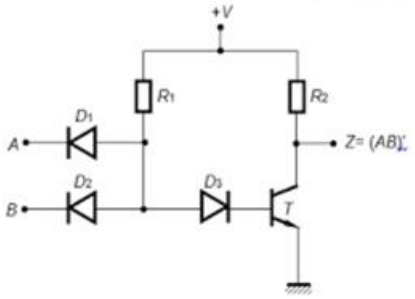
Evolução das famílias lógicas



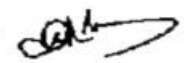
DCTL



RTL



DTL



Evolução das famílias lógicas : DTL → TTL

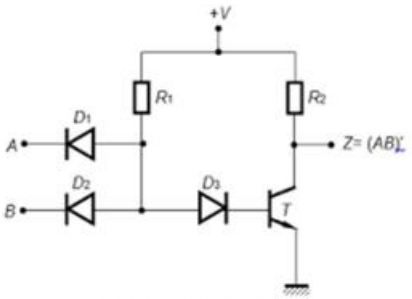
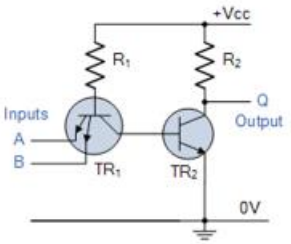
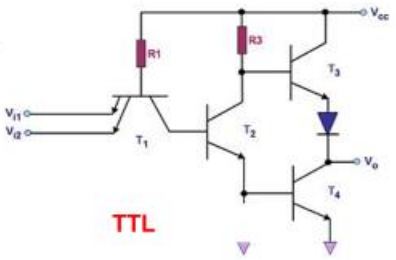


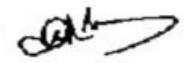
Fig. 3.2 Two-input DTL NAND gate

DTL

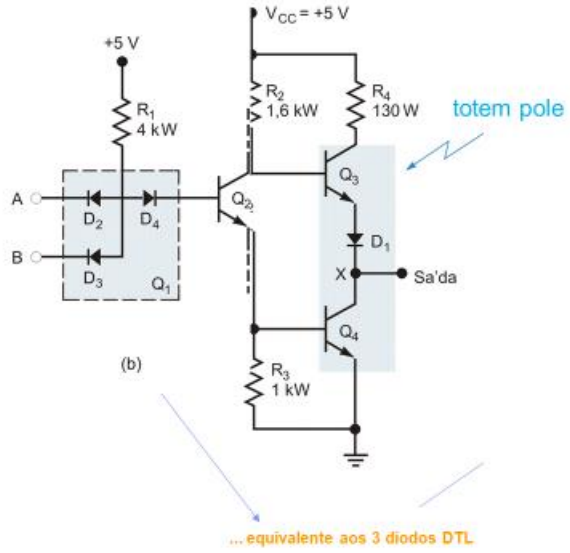




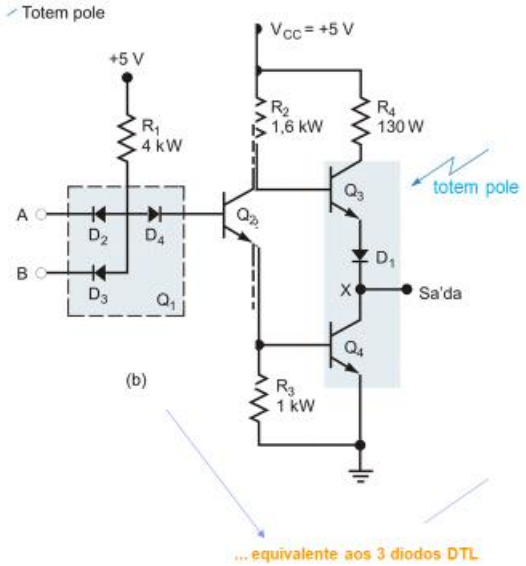
TTL

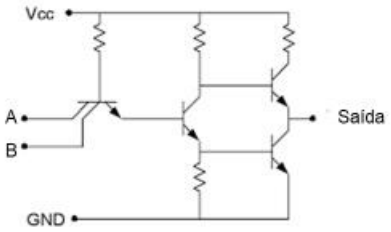


Porta NAND TTL



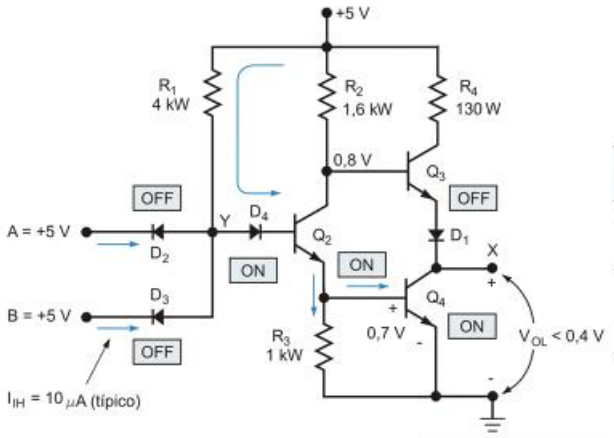
Porta NAND TTL





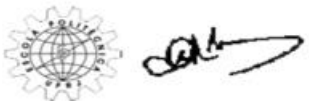
A	B	Saída
0	0	1
0	1	1
1	0	1
1	1	0

Chaveamento TTL

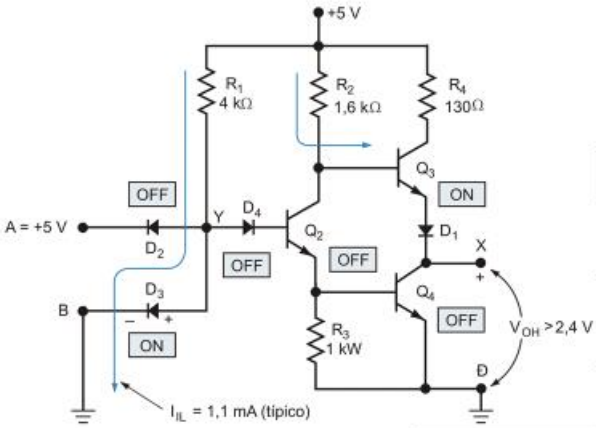


(a) Saída em nível BAIXO

Condições de entrada	Condições de saída
A e B estão ambas em nível ALTO (≥ 2 V)	Q_3 OFF
As correntes de entrada são muito baixas I_{IH} = 10 μA	Q_4 ON, logo, V_X está em nível baixo (≤ 0,4 V)



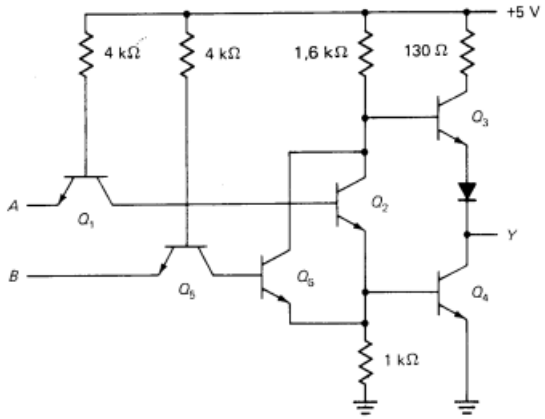
Chaveamento TTL



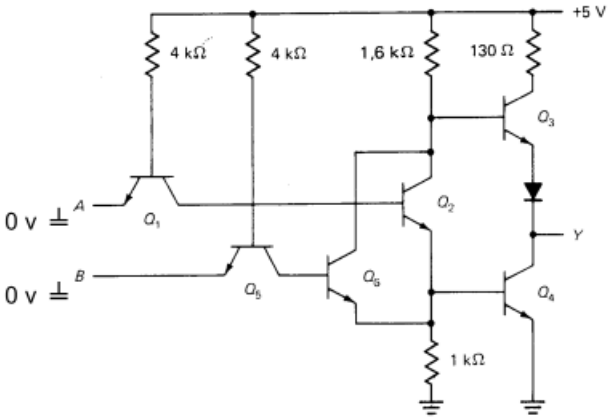
(b) Saída em nível ALTO

Condições de entrada	Condições de saída
A e B estão ambas em nível ALTO (≤ 0,8 V)	Q_4 OFF
A corrente flui para GND através do terminal de entrada em nível baixo. I_{IL} = 1,1 mA	Q_3 atua como um seguidor de emissor e V_{OH} ≥ 2,4 V, geralmente 3,6 V

Que porta é esta ?

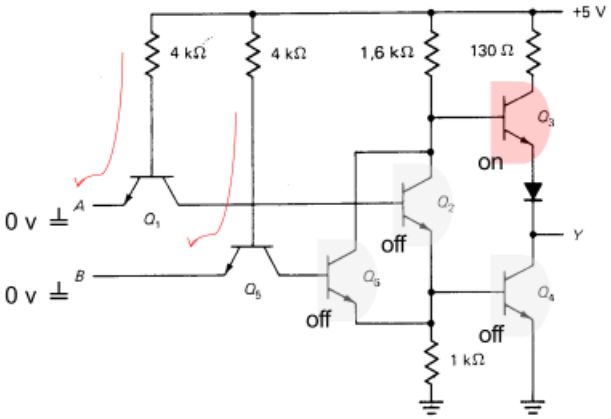


Que porta é esta ?



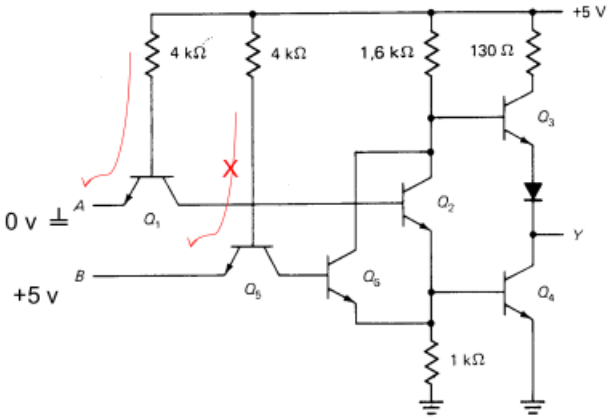
A	B	Y
0	0	
0	1	
1	0	
1	1	

Que porta é esta ?



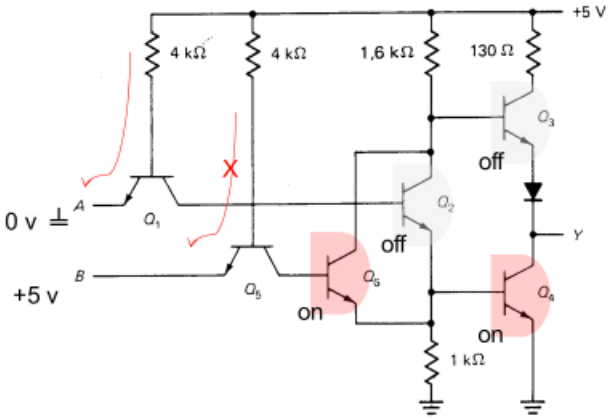
A	B	Y
0	0	1
0	1	
1	0	
1	1	

Que porta é esta ?



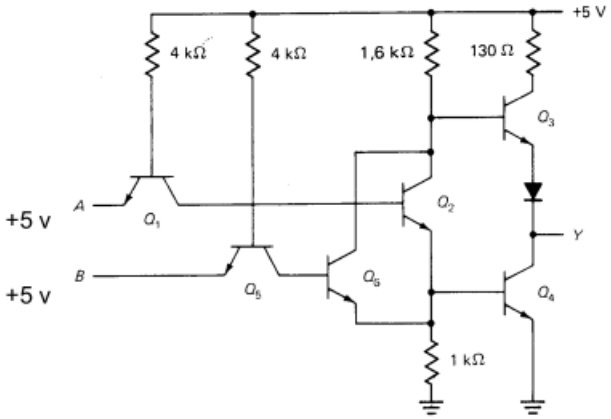
A	B	Y
0	0	1
0	1	
1	0	
1	1	

Que porta é esta ?



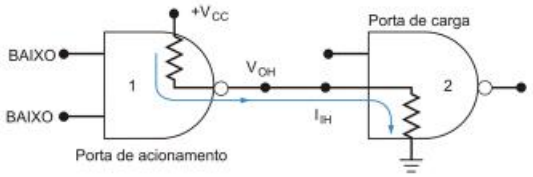
A	B	Y
0	0	1
0	1	0
1	0	
1	1	

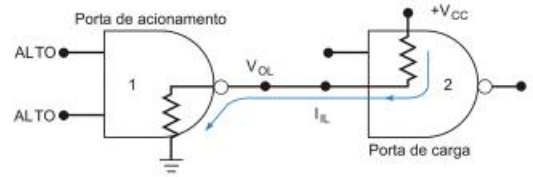
Que porta é esta ? NOR

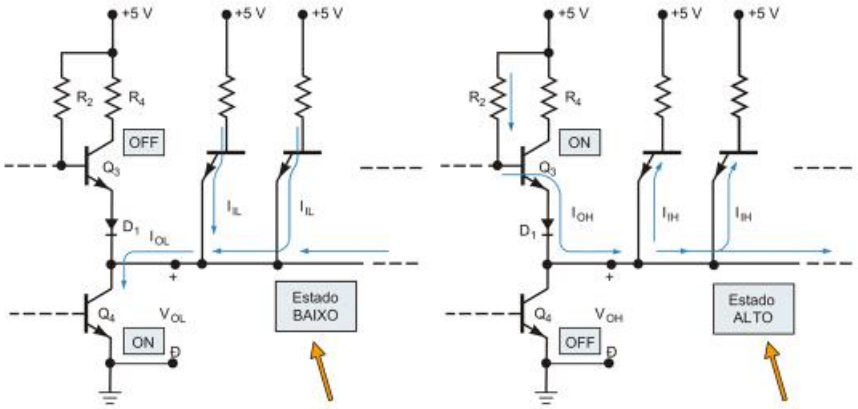


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Correntes nas interligações de portas TTL



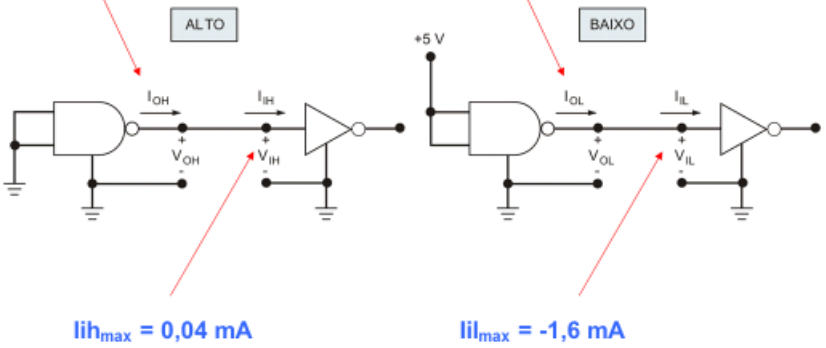




Correntes nas interligações de portas TTL

Ioh_{max} = 0,4 mA

Iol_{max} = -16 mA



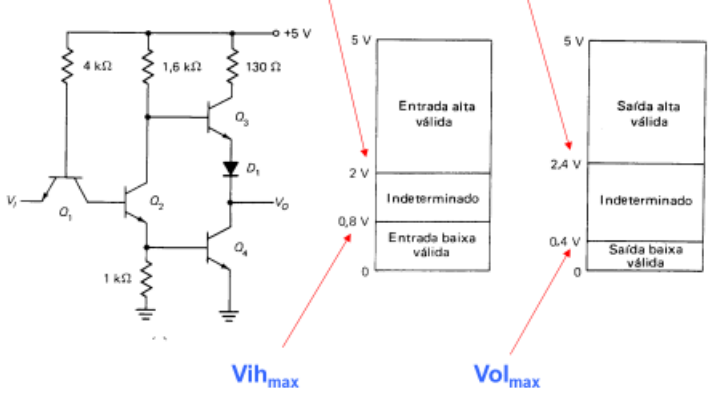
Iih_{max} = 0,04 mA

Iil_{max} = -1,6 mA

Tensão nos níveis lógicos

Vih_{min}

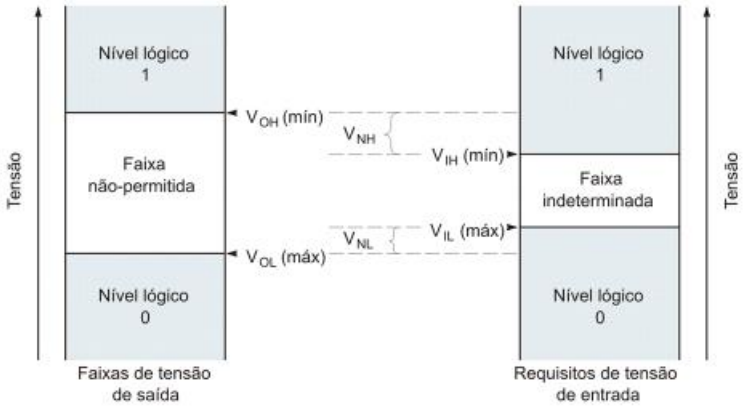
Voh_{min}



Vih_{max}

Vol_{max}

Margem de ruído



Características da Família TTL

A família TTL, como qualquer outra famíla lógica, têm uma série de características que lhe são peculiares. Apresentamos a seguir algumas delas :

- *Tensão de Alimentação*:

Família	Mínima	Típica	Máxima
TTL	4,5 V	5 V	5,5 V

- *Tensão de Entrada**: $V_{IL,\,máx}$ = 0,8 V $V_{IH,\,máx}$ = 2 V
- *Tensão de Saída**: $V_{OL,\,máx}$ = 0,4 V $V_{OH,\,máx}$ = 2,4 V
- *Correntes de Entrada**: $I_{IL,\,MÁX}$ = -1,6 mA $I_{IH,\,MÁX}$ = 40 mA
- *Correntes de Saída**: $I_{OL,\,MÁX}$ = 16 mA $I_{OH,\,MÁX}$ = -400 mA

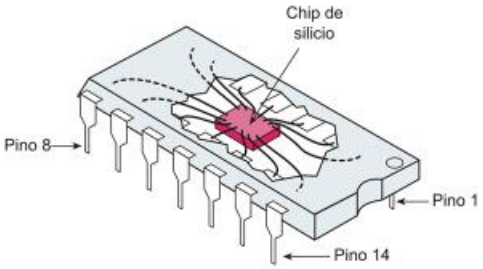
Fan-out → 10

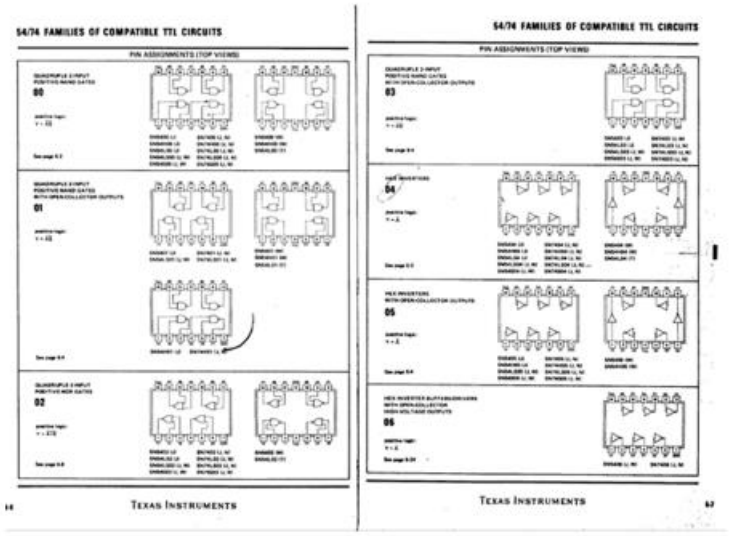
Margem de ruído → 0,4 V

Atraso por porta → 10 ηs

Consumo por porta → 10 mW

Circuitos integrados : CIs e chips





54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

00

01

02

14 TEXAS INSTRUMENTS

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

03

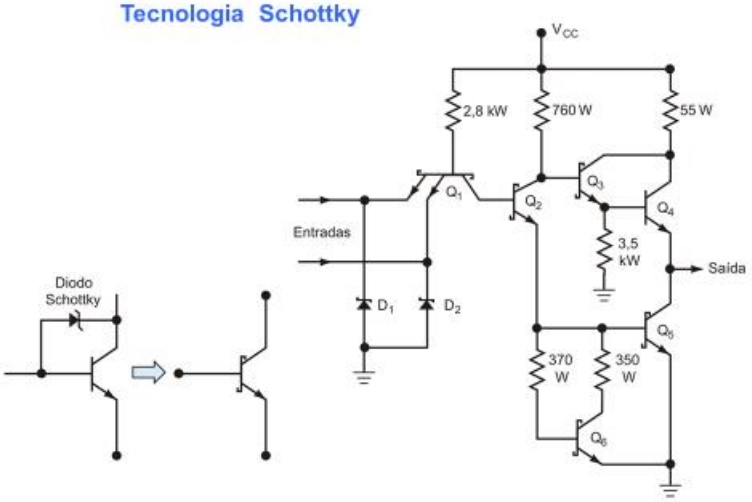
04

05

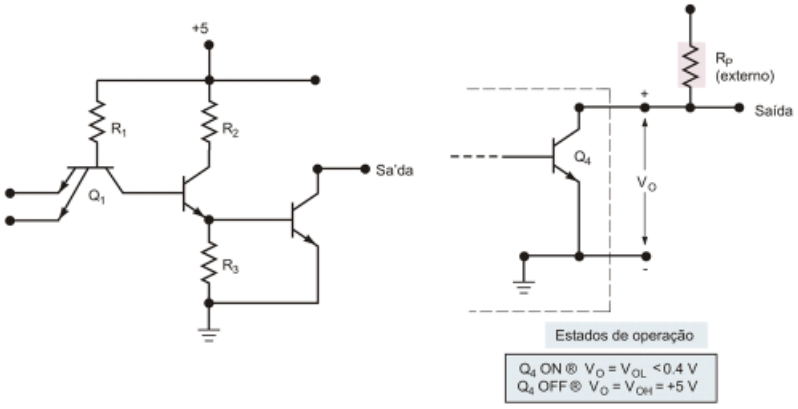
06

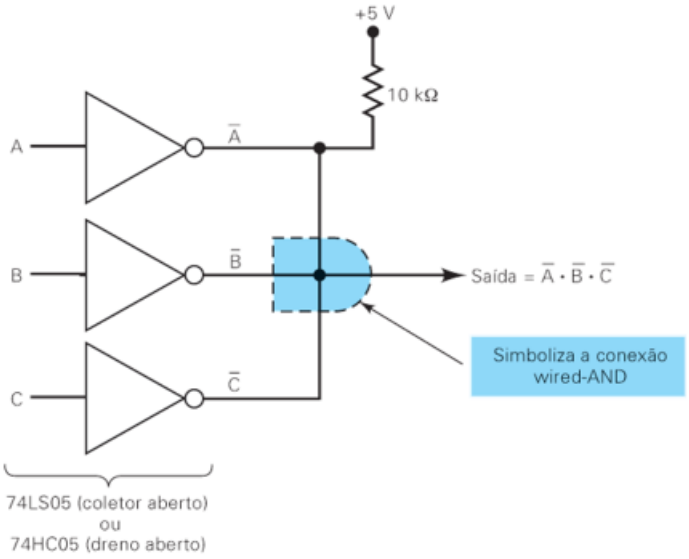
TEXAS INSTRUMENTS 63

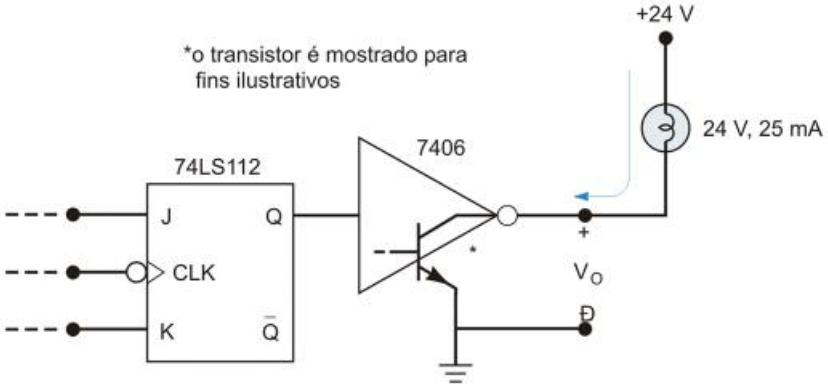
Tecnologia Schottky



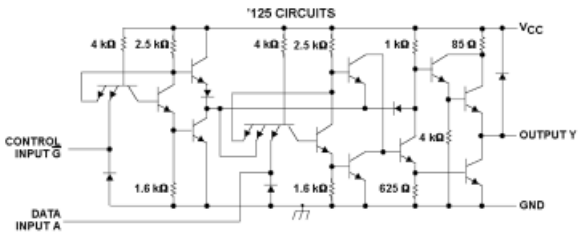
Porta open-collector OC (coletor aberto)

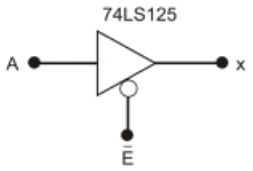



+5 V
10 kΩ
A
B
C
$\overline{A}$
$\overline{B}$
$\overline{C}$
Saída = $\overline{A} \cdot \overline{B} \cdot \overline{C}$
Simboliza a conexão wired-AND
74LS05 (coletor aberto)
ou
74HC05 (dreno aberto)

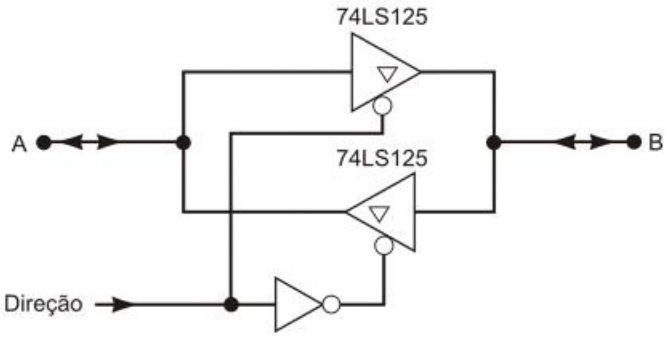

+24 V
*o transistor é mostrado para fins ilustrativos
24 V, 25 mA
74LS112
7406
J
CLK
K
Q
$\overline{Q}$
+
V_O
–

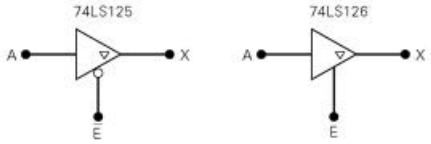
Porta 3-state (three-state)



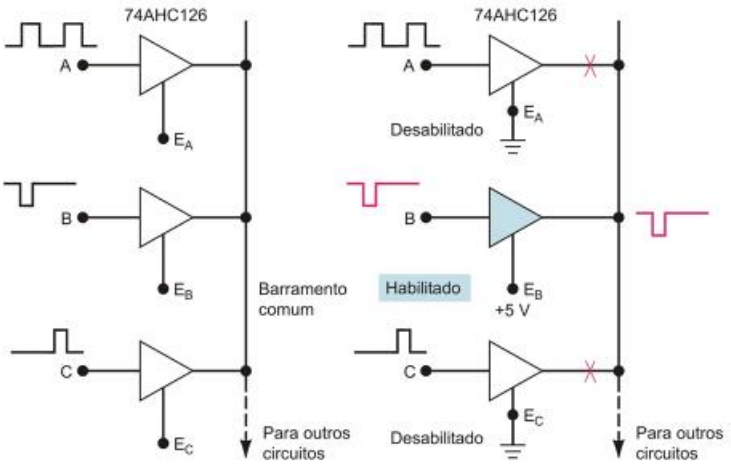


Ē	x
0	A
1	Alta impedância

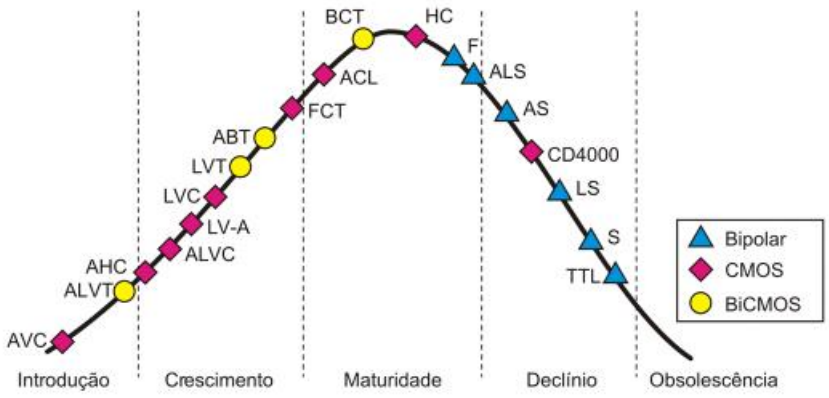




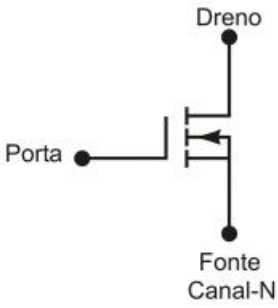
Barramentos

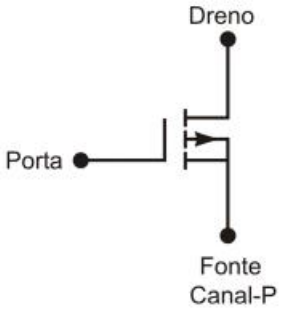


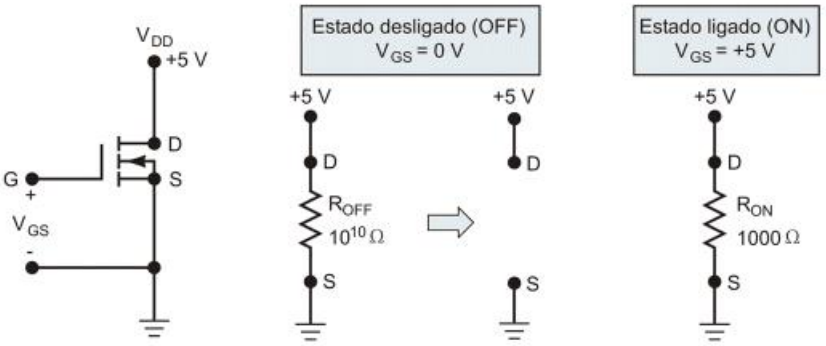
Ciclo de vida das famílias lógicas (Texas Instruments)



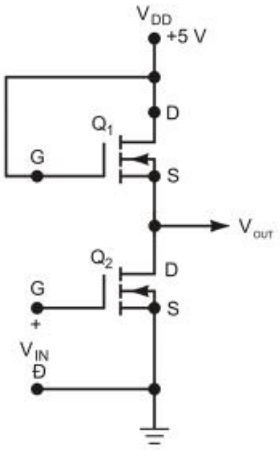
Tecnologia MOS







Tecnologia NMOS

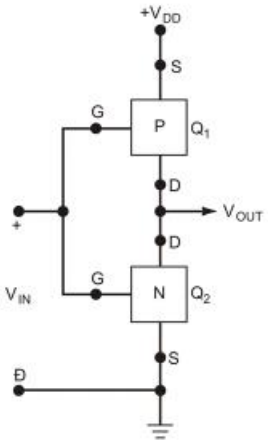


(a)

V_{IN}	Q_1	Q_2	$V_{OUT} = \overline{V_{IN}}$
0 V (lógico 0)	R_{ON} = 1,00 kΩ	R_{OFF} = 10^{10} Ω	+5 V (lógico 1)
+5 V (lógico 1)	R_{ON} = 1,00 kΩ	R_{ON} = 1 kΩ	+0,05 V (lógico 0)

(b)

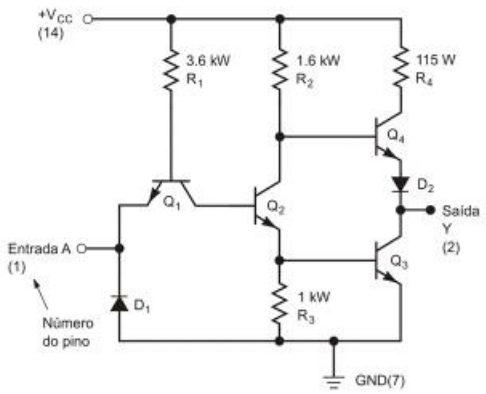
Tecnologia CMOS



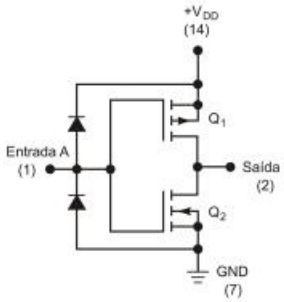
V_{IN}	Q_1	Q_2	V_{OUT}
$+V_{DD}$ (1 lógico)	OFF $R_{OFF} = 10^{10}$ Ω	ON R_{ON} = 1 kΩ	≃ 0 V
0 V (0 lógico)	ON R_{ON} = 1 kΩ	OFF $R_{OFF} = 10^{10}$ Ω	≃ $+V_{DD}$

$V_{OUT} = \overline{V_{IN}}$

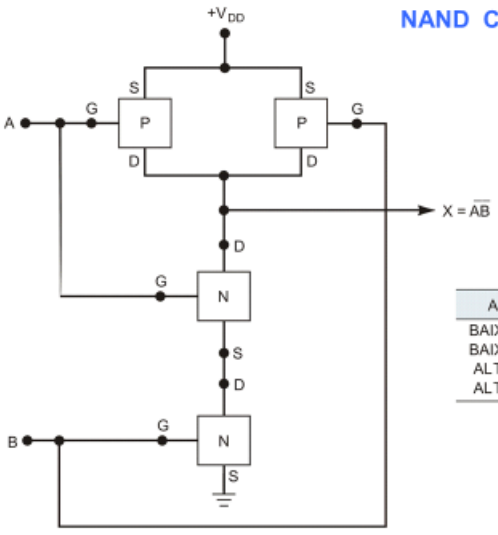
NOT TTL



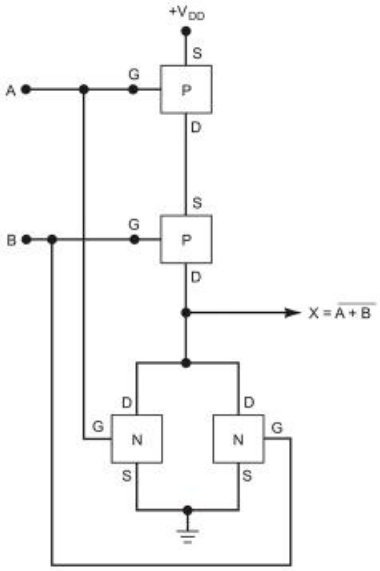
NOT CMOS



NAND CMOS



A	B	X
BAIXO	BAIXO	ALTO
BAIXO	ALTO	ALTO
ALTO	BAIXO	ALTO
ALTO	ALTO	BAIXO



NOR CMOS

A	B	X
BAIXO	BAIXO	ALTO
BAIXO	ALTO	BAIXO
ALTO	BAIXO	BAIXO
ALTO	ALTO	BAIXO

Leitura indicada

Maini, A.K. "Digital Electronics – Principles and Integrated Circuits"

a) Sec. 3.1 – 3.10 , pgs. 71 – 93

b) Sec. 4.1 – 4.7 , pgs. 107 – 146

3 Logic Gates and Related Devices

LEARNING OBJECTIVES

After completing this chapter, you will learn the following:

- Difference between positive and negative logic.
- Functional description of basic and derived logic gates.
- Truth table.
- Building logic gates with more than two inputs using basic logic gates.
- Logic gates with open collector/drain outputs.
- Universal gates.
- Schmitt and INHIBIT gates.
- Gates with complementary outputs.
- Comparison between logic gates, buffers, and transceivers.
- IEEE/ANSI symbols for logic gates.
- Application relevant information on popular type numbers.

4 Logic Families

LEARNING OBJECTIVES

After completing this chapter, you will learn the following:

- Significance of logic family for digital circuit designers.
- Common logic families.
- Parameters defining a logic family.
- Comparison of different logic families.
- Transistor transistor logic (TTL) and its sub-families.
- CMOS logic family.
- PMOS and NMOS logic families.
- Emitter coupled logic (ECL) family.
- Bipolar-CMOS (BiCMOS) logic family.
- Integrated injection logic (I^2L) family.
- Guidelines to using TTL and CMOS devices.
- Interface aspects of different logic families.